CLAIM AMENDMENTS

Please amend Claims 1 as follows:

1. (Currently Amended) A semiconductor device provided at least with source and drain regions of a first conductivity type and a semiconductor layer including a channel region between said source and drain regions, an insulating layer covering at least said channel region, and a gate electrode arranged close to said insulating layer,

wherein said channel region comprises a first channel area of a second conductivity type opposite to the first conductivity type and of low resistivity arranged close to said insulating layer, a second channel area of the first conductivity type and of a high resistivity arranged close to said first channel area, and a third channel area of the second conductivity type arranged close to said second channel area, said third channel area is arranged close to an additional insulating layer, and an electrically neutral area is formed in said third channel area at a side adjacent to said additional insulating ~~area~~ layer.

2. (Cancelled).

3. (Original) A semiconductor device according to claim 1, wherein said second channel area is depleted at least when the voltage applied to the gate electrode is zero.

4. (Original) A semiconductor device according to claim 1, wherein the thickness of said first channel area is larger than the mean free path of the drifting carriers.

5. (Previously Presented) A semiconductor device according to claim 1, wherein said additional insulating layer is an insulative substrate.

6. (Cancelled)

7. (Original) A semiconductor device according to claim 5, wherein said second channel area is depleted at least when the voltage applied to the gate electrode is zero.

8. (Original) A semiconductor device according to claim 5, wherein the thickness of said first channel area is larger than the mean free path of the drifting carriers.

9. - 10. (Cancelled)

11. (Withdrawn) A semiconductor device provided at least with a semiconductor layer including source and drain areas of a first conductive type and of a high impurity concentration and a channel area positioned between said source and drain areas, an insulation layer covering at least said channel area, and a gate electrode positioned close to said insulation layer, wherein said channel area at least comprises a first

channel area of a low resistance, positioned close to said insulation layer and having a second conductive type opposite to said first conductive type, and a second channel area of a high resistance, having said first conductive type and positioned adjacent to said first channel area, and further comprises a substrate of the second conductive type, positioned adjacent to said second channel area, said semiconductor device constituting an integrated circuit including an MIS transistor comprising a third channel area of the first conductive type having an impurity concentration different from the second channel area, positioned between the first and second channel areas.

12. - 13. (Cancelled)

14. (Withdrawn) A semiconductor device according to claim 1, wherein the impurity concentration of said source and drain areas is within a range of 10^{18} to 10^{21} cm^{-3}.

15. (Withdrawn) A semiconductor device according to claim 1, wherein the impurity concentration of said first channel area is within a range of 10^{15} to 10^{19} cm^{-3}.

16. (Withdrawn) A semiconductor device according to claim 1, wherein the impurity concentration of said second channel are is 1×10^{17} cm^{-3} or lower.

17. (Withdrawn) A semiconductor device according to claim 1, wherein said first conductive type is n-type.

18. (Withdrawn) A semiconductor device according to claim 1, wherein said second conductive type is p-type.

19. (Withdrawn) A semiconductor device according to Claim 1, wherein the impurity concentration of said third channel area is within a range of 1014 to 10^{18} cm^{-3}

20. (Withdrawn) A semiconductor device according to Claim 1, further comprising an additional gate electrode on said third channel across said additional insulating layer.

21. (Withdrawn) A semiconductor device according to claim 11, wherein the impurity concentration of said third channel area is higher than that of said second area.

22. (Withdrawn) A semiconductor device according to Claim 11, wherein the impurity concentration of said third channel area is lower than that of said second area.

23. (Cancelled).

24. (Withdrawn) A semiconductor device according to Claim 23, wherein said MIS transistor is of an enhancement type.

25. (Withdrawn) A semiconductor device according to Claim 11, wherein an impurity concentration in said source and drain regions is 10^{18}-10^{21} cm^{-3}.

26. (Withdrawn) A semiconductor device according to Claim 11, wherein the impurity concentration in said first channel area is 10^{15}-10^{19} cm^{-3}.

27. (Withdrawn) A semiconductor device according to Claim 11, wherein the impurity concentration in said second or third channel area is not greater than 10^{17} cm^{-3}.

28. (Withdrawn) A semiconductor device according to Claim 11, wherein the first conductivity type is n.

29. (Withdrawn) A semiconductor device according to Claim 11, wherein the second conductivity type is p.

30. (Withdrawn) A semiconductor device according to Claim 11, wherein the impurity concentration in said substrate is 10^{14}-10^{18} cm^{-3}.

31. (Withdrawn) A semiconductor device provided at least with source and drain regions of a first conductivity type and of a high impurity concentration, a semiconductor layer including a channel region between said source and drain regions, an insulating layer at least on said semiconductor layer, and a gate electrode on said insulating layer, wherein at least said semiconductor layer comprises a first area of low resistivity and of a second conductivity type opposite to the first conductivity type adjacent to said insulating layer, a third area of the first conductivity type, having an impurity concentration different than the second channel area, adjacent to the first area, a second area of the first conductivity type adjacent to said third area, and a substrate of the second conductivity type adjacent to said second area.

32. (Withdrawn) A semiconductor device according to claim 31, wherein the impurity concentration of said third area is higher than that of said second area.

33. (Withdrawn) A semiconductor device according to Claim 31, wherein the impurity concentration of said third area is lower than that of said second area.

34. (Cancelled)

35. (Withdrawn) A semiconductor device according to Claim 34, wherein said MIS transistor is of an enhancement type.

36. (Withdrawn) A semiconductor device according to Claim 31, wherein an impurity concentration in said source and drain regions is 1018-1021 cm-3.

37. (Withdrawn) A semiconductor device according to Claim 31, wherein the impurity concentration in said first area is 10^{15}-10^{19} cm^{-3}.

38. (Withdrawn) A semiconductor device according to Claim 31, wherein the impurity concentration in said second or third area is not greater than 10^{17} cm^{-3}.

39. (Withdrawn) A semiconductor device according to Claim 31, wherein the first conductivity type is n.

40. (Withdrawn) A semiconductor device according to Claim 31, wherein the second conductivity type is p.

41. (Withdrawn) A semiconductor device according to Claim 31, wherein the impurity concentration in said substrate is 10^{14}-10^{18} cm^{-3}.